



Field Service Bulletin F9800_01_01

Products Affected: F9800_01_01

Description: When using CPU boards, which do not have the “Master Reset” ECO, the Master Reset circuitry can sometimes malfunction causing the F-9800 tuning elements to be incorrectly set.

Recommendations: JPS recommends the ECO be added to all units.

Conditions: When ECO # 9112-09 is not performed on an F9800, the unit will display operation failures during the BIT test as described as follows.

F9800 Timing Analysis

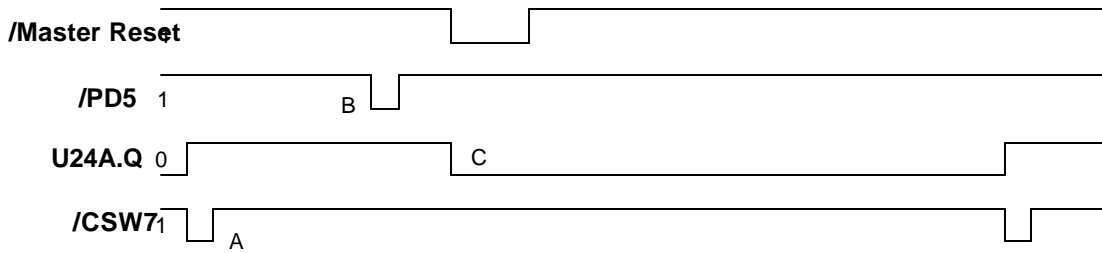
When using the older CPU boards, which do not have the “Master Reset” ECO the Master Reset circuitry can sometimes, malfunction causing the F-9800 tuning elements to be incorrectly set. The Master Reset circuitry centers around a 74HC123 (U24) on the CPU board. In the original design, U24A would serve to automatically initiate a Master Reset pulse whenever its “A” input (/CSW7) was active. The Master Reset pulse would occur approximately 23 mS after the /CSW7 activity began. The second half of the 74HC123 is used to create the Master Reset pulse itself. Its “A” input is tied to U24A such that the high-to-low transition after 23 mS causes a Master Reset pulse to be generated. The “B” input to U24B (/PD5) is a signal, which comes directly from the CPU. /PD5 is used whenever the CPU wishes to initiate a Master Reset pulse manually.

This original configuration was abandoned later as it was found to occasionally cause a conflict where a Master Reset pulse was generated while the tuning elements were still in a state of transition. The change simply eliminated U24A from the circuit. Using this method all Master Reset pulses are initiated by the CPU.

On CPU boards which have not been modified, the /PD5 pulse from the CPU has no effect since U24A is controlling the Master Reset pulse. The signal timing looks like Figure 1.



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CPU Board Master Reset Operation Without ECO

- A. /CSW7 becomes active with a series of 10 pulses as the tuning elements are being set up. This series of pulse at this time U24A.Q becomes active (going high).
- B. After the tuning elements have been set up, the CPU issues a pulse on /PD5 to trigger a Master Reset pulse. Since this pulse has no effect.
- C. U24A.Q transitions from high-to-low causing a Master Reset pulse to be generated.

Figure 1

The net effect is that the CPU is no longer controlling the Master Reset pulse. Under normal operation, this is not a problem. The problem occurs when the F-9800 is running its BITE test. Under this condition, there is sometimes a conflict in timing where the Master Reset pulse is still active when the tuning elements are being changed. This causes the elements to be mistuned, which in turn may cause a BITE failure. The problem can sometimes be heard as a “skipping” in the tuning relays during BITE.

Since it is possible to send frequency change information to the F-9800 faster than it can reliably change its tuning elements the following recommendations are made:

The F-9800 should not be commanded to change frequency faster than once every 200 milliseconds.

There should be a delay of at least 200 milliseconds after giving a frequency change command before giving a “Key” or “Unkey” command. This is because a Master Reset pulse is generated by the “Keying” command.

Required Equipment: Screwdriver, soldering iron, exacto blade.

Procedure/Corrective Actions: Please see page two for the systematic procedure to add the ECO.

Procedure:

- 1) Remove the top cover of the F9800.
- 2) Remove the seven screws from the CPU board.



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- 3) Cables J10 and P12 do not have to be removed; the board can be flipped over while they are attached.
- 4) Turn the board over, locate the area where the changes are required, please see Figure 2.

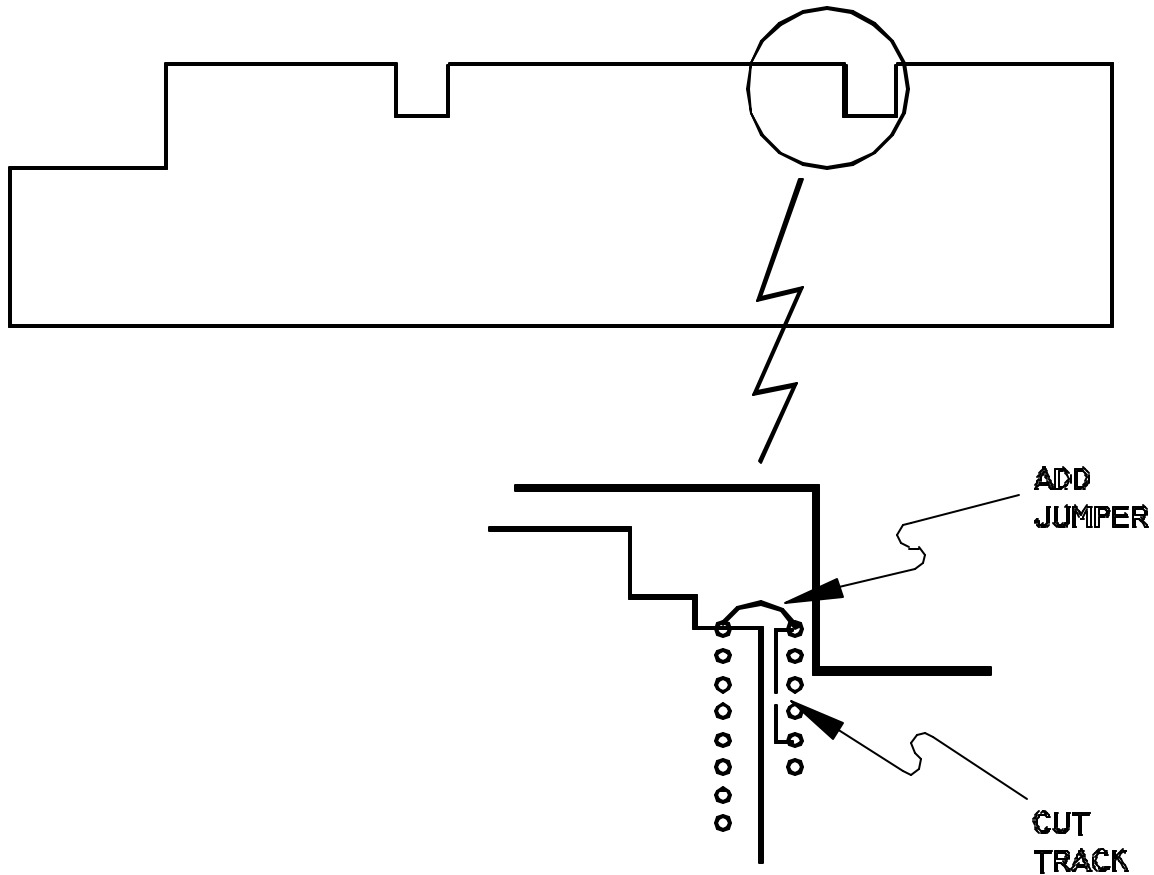


Figure 2

- 5.) Cut the track between pin 9 and pin 13 of U24 as shown above.
- 6.) Add a jumper between pin 9 and pin 8 of U24 as shown above.
- 7.) Replace the board back into the chassis.
- 8.) Re-connect the cables
- 9.) Replace the screws, which hold the board.
- 10.) Replace the cover.



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Units Pending ECO: Gray lines ECO performed at JPS under RMA's.

Test Date	Serial Numbers
6/20/01	509
6/21/01	510
6/21/01	511
6/11/01	512
6/21/01	513
6/20/01	514
6/25/01	515
6/13/01	516
6/13/01	517
6/4/01	518
6/26/01	519
6/27/01	520
6/25/01	521
6/19/01	522
6/13/01	523
6/14/01	524
6/28/01	525
6/28/01	526
6/20/01	527
6/7/01	528
6/18/01	529
6/5/01	530
6/7/01	531
6/12/01	532
6/18/01	533
6/13/01	534
7/2/01	535
6/14/01	536
6/12/01	537
6/27/01	538
6/13/01	539
6/18/01	540
6/25/01	541
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6/27/01	544
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6/21/01	550
6/26/01	551
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6/26/01	553
6/11/01	554
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5/31/01	557
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Assistance: For further assistance or information please contact the customer service department at JPS Communications, Inc.